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MATERIALS SUITABLE FOR SHALLOW TRENCH ISOLATION

BACKGROUND OF THE INVENTION

FIELD OF THE INVENTION

The present invention relates to semiconductor device fabrication and more specifically to a method and material for forming shallow trench isolation structures in integrated circuits.

DESCRIPTION OF THE RELATED ART

In the semiconductor industry, there is a continuing trend toward higher device densities. To achieve these high densities there has been continuing efforts toward scaling down device dimensions at submicron levels on semiconductor wafers. In order to accomplish such high device packing density, smaller and smaller feature sizes are required. This may include the width and spacing of interconnecting lines, spacing and diameter of contact holes, and the surface geometry such as corners and edges of various features. The trend in modern integrated circuit manufacture is to produce semiconductor devices, including, for example, MOSFETs, other types of transistors, memory cells, and the like, that are as small as possible. It is also advantageous to reduce the scale of the isolation regions that are formed between the devices. Although the fabrication of smaller devices and isolation regions allows more devices to be placed on a single monolithic substrate for the formation of relatively large circuit systems in a relatively small die area, this downscaling can result in a number of performance degrading effects.

To achieve proper isolation between devices in integrated circuits, a technique known as Shallow Trench Isolation (STI) is used. As the elements incorporated into a semiconductor device are integrated to a high degree, there is a growing tendency to increasingly use the STI method as a method of forming an isolation layer as compared with a local oxidation of silicon (LOCOS) method. LOCOS involves depositing a non-oxidizable mask, such as silicon nitride over a thin layer of oxide grown on a blank silicon wafer. The mask is patterned using photolithography and then the wafer is thermally oxidized. Following oxidation, mesa-like regions of silicon are formed that are surrounded by silicon oxide insulation. The active devices are then formed using the silicon mesas. Another technique is deep trench isolation (DTI). DTI has primarily been used for forming isolation regions between bipolar transistors. STI involves forming trenches in a layer of silicon and then filling the trenches with silicon oxide. The trenches can be lined with a silicon oxide liner formed by a thermal oxidation process and then filled with additional silicon oxide or another material, such as polysilicon. These filled trenches define the size and placement of the active regions. The use of STI significantly shrinks the area needed to isolate transistors better than local oxidation of silicon. The STI method comprises etching a substrate to form trenches for isolation, and filling the trenches with an insulating layer. Thus, each isolated region is separated by the trenches and the insulating layer filled therein. As device packing density increases, STI becomes an inevitable feature of the integrated circuit. In deep sub-micron integration, STI with higher aspect ratios (height/width) are required, which may be as small as 10 to 90 nm or even smaller in next generation devices. Accordingly, there exists a need in the art for improved isolation between semiconductor devices and for techniques of fabricating improved isolation regions along with semiconductor devices. Clearly, there is a need to develop a material that can fill such narrow features without cracking and voids. Furthermore, the desired dielectric materials need to

be able to withstand processing steps, such as high temperature anneal, chemical mechanical polishing (CMP), RIE etch, HF wet etch and cleaning steps.

In most cases, it is critical to have STI features completely filled with the dielectric materials without cracking and voids. Typically, dielectric materials are deposited by chemical vapor deposition (CVD) or by spin-on processes. The existing CVD (SACVD, LPCVD, HDP CVD and et. al.) and atomic layer deposition (ALD) approaches often lead to voiding inside of the trenches; and/or elaborative deposition/etch steps that are not feasible for gap-filling narrow features.

Using prior techniques, deep and narrow trenches are difficult to etch. Several undesirable effects may arise from devices employing high aspect ratio STI. These include damage to the substrate due to excessive etching and severe microloading effects between dense and open trenches. Additionally, problems may result from incomplete clearing of etch by-product residue at the bottom of narrow trenches. Typical semiconductor devices are formed using active regions of a wafer. The active regions are defined by isolations regions used to separate and electrically isolate adjacent semiconductor devices. For example, in an integrated circuit having a plurality of metal oxide semiconductor field effect transistors (MOSFETs), each MOSFET has a source and a drain that are formed in an active region of a semiconductor layer by implanting N-type or P-type impurities in the layer of semiconductor material. Disposed between the source and the drain is a channel (or body) region. Disposed above the body region is a gate electrode. The gate electrode and the body are spaced apart by a gate dielectric layer.

Relatively narrow STI regions (e.g., about 180 Ǎ or less) formed using

conventional techniques have a tendency lose their ability to isolate adjacent devices. Accordingly, there exists a need in the art for improved isolation between semiconductor devices and for techniques of fabricating improved isolation regions along with semiconductor devices.

Spin-on glasses and spin-on polymers such as silicate, silazane, silisequioxane or siloxane generally exhibit good gap-fill properties. The silicon oxide films are formed by applying a silicon-containing pre-polymer onto a substrate followed by a bake and a high temperature anneal. Historically, the spin-on approach has been hampered by the unacceptable film cracking inside narrow trenches as the result of high film shrinkage after high temperature anneal which exceed 750 °C. Film cracking also lead to undesirable high HF wet etch rate and un-reliable yield issues.

Thus, there exists a need in the art for a dielectric spin-on materials that provides crack-free and void-free gap-fill of narrow features at process temperature higher than 750 °C. These materials need to have a very desirable degree of wet etch resistance and hardness which is comparable to PECVD oxide.

SUMMARY OF THE INVENTION

The invention provides a method of producing a silica dielectric film comprising

(a) preparing a composition comprising a silicon containing pre-polymer, optionally water, and optionally a metal-ion-free catalyst selected from the group consisting of onium compounds and nucleophiles;

(b) coating a substrate with the composition to form a film,

(c) crosslinking the composition to produce a gelled film, and

(d) heating the gelled film at a temperature of from about 750 °C to about 1000 °C and for a duration effective to remove substantially all organic moieties and to produce a substantially crack-free, and substantially void-free silica dielectric film.

The invention also provides a method of forming isolation structures in a semiconductor substrate comprising:

a) etching trenches in a semiconductor substrate, thereby forming substantially unetched areas of said substrate between said trenches;

b) depositing a conformal fill composition that substantially fills said trenches and to form a film, said composition comprising a silicon containing pre-polymer, optionally water, and optionally a metal-ion-free catalyst selected from the group consisting of onium compounds and nucleophiles;

(c) crosslinking the composition to produce a gelled film, and

(d) heating the gelled film at a temperature of from about 750 °C to about 1000 °C and for a duration effective to remove substantially all organic moieties and to produce a substantially crack-free, and substantially void-free silica dielectric film.

e) optionally planarizing said silica dielectric film.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

Silicon-based dielectric films are prepared from a composition comprising a suitable silicon containing pre-polymer, optionally blended with water and/or a metal-ion-free catalyst which may be an onium compound or a nucleophile. One or more optional solvents and/or other components may also be included. The dielectric precursor composition is applied to a substrate suitable, e.g., for production of a semiconductor device, such as an integrated circuit ("IC"), by any art-known method to form a film. The composition is then crosslinked, such as by heating to produce a gelled film. The gelled film is then heated at a higher temperature to remove substantially all of the organic moieties in the film and to produce a substantially crack-free, and void-free silica dielectric film.

The films produced by the processes of the invention have a number of advantages over those previously known to the art, including substantially crack-free and substantially void free gap-fill, improved density, mechanical strength, that enables the produced film to withstand the further processing steps required to prepare a semiconductor device on the treated substrate, and excellent wet etch resistance which is comparable to PECVD silicon oxide.

The resulting silica film typically has a density of from about 2 to about 2.3 g/milliliter, and more typically from about 2.1 to about 2.3 g/milliliter.

It should be understood that the term gelling refers to condensing, or polymerization, of the combined silica-based precursor composition on the substrate after deposition.

Dielectric films are prepared from suitable compositions applied to substrates in the fabrication of integrated circuit devices. Art-known methods for applying the dielectric precursor composition, include, but are not limited to, spin-coating, dip coating, brushing, rolling, and/or spraying. Prior to application of the base materials to form the dielectric film, the substrate surface is optionally prepared for coating by standard, art-known cleaning methods. The coating is then processed to achieve the desired type and consistency of dielectric coating, wherein the processing steps are selected to be appropriate for the selected precursor and the desired final product. Further details of the inventive methods and compositions are provided below.

A "substrate" as used herein includes any suitable composition formed before a silica film of the invention is applied to and/or formed on that composition. For example, a substrate is typically a silicon wafer suitable for producing an integrated circuit, and the base material from which the silica film is formed is applied onto the substrate by conventional methods. Suitable substrates for the present invention non-exclusively include films, glass, ceramic, plastic, composite materials, silicon and compositions containing silicon such as crystalline silicon, polysilicon, amorphous silicon, epitaxial silicon, silicon dioxide ("SiO_2"), silicon nitride, silicon oxide, silicon oxycarbide, silicon carbide, silicon oxynitride, organosiloxanes, organosilicon glass, fluorinated silicon glass, and semiconductor materials such as gallium arsenide ("GaAs"), and mixtures thereof. In other embodiments, the substrate comprises a material common in the packaging and circuit board industries such as silicon, glass, and polymers. The circuit board made up of the present composition will have mounted on its surface patterns for various electrical conductor circuits. The circuit board may include various reinforcements, such as woven non-conducting fibers or glass cloth. Such circuit boards may be single sided, as well as double sided.

On the surface of the substrate is an optional pattern of raised lines, such as oxide, nitride or oxynitride lines which are formed by well known lithographic techniques. Suitable materials for the lines include silicon oxide, silicon nitride, and silicon oxynitride. Other optional features of the surface of a suitable substrate include an oxide layer, such as an oxide layer formed by heating a silicon wafer in air, or more preferably, an SiO_2 oxide layer formed by chemical vapor deposition of such art-recognized materials as, e.g., plasma enhanced tetraethoxysilane oxide ("PETEOS"), plasma enhanced silane oxide ("PE silane") and combinations thereof, as well as one or more previously formed silica dielectric films.

The silica film of the invention can be applied so as to cover and/or lie between such optional electronic surface features, e.g., circuit elements and/or conduction pathways that may have been previously formed features of the substrate. Such optional substrate features can also be applied above the silica film of the invention in at least one additional layer, so that the low dielectric film serves to insulate one or more, or a plurality of electrically and/or electronically functional layers of the resulting integrated circuit. Thus, a substrate according to the invention optionally includes a silicon material that is formed over or adjacent to a silica film of the invention, during the manufacture of a multilayer and/or multicomponent integrated circuit. In a further option, a substrate bearing a silica film or films according to the invention can be further covered with any art known non-porous insulation layer, e.g., a glass cap layer.

The crosslinkable composition employed for forming silica dielectric films according to the invention includes one or more silicon-containing prepolymers that are readily condensed. It should have at least two reactive groups that can be

hydrolyzed. Such reactive groups include, alkoxy (RO), acetoxy (AcO), etc. Without being bound by any theory or hypothesis as to how the methods and compositions of the invention are achieved, it is believed that water hydrolyzes the reactive groups on the silicon monomers to form Si-OH groups (silanols). The latter will undergo condensation reactions with other silanols or with other reactive groups, as illustrated by the following formulas:

$$\text{Si-OH} + \text{HO-Si} \rightarrow \text{Si-O-Si} + H_2O$$
$$\text{Si-OH} + \text{RO-Si} \rightarrow \text{Si-O-Si} + \text{ROH}$$
$$\text{Si-OH} + \text{AcO-Si} \rightarrow \text{Si-O-Si} + \text{AcOH}$$
$$\text{Si-OAc} + \text{AcO-Si} \rightarrow \text{Si-O-Si} + Ac_2O$$

R = alkyl or aryl

Ac = acyl (CH_3CO)

These condensation reactions lead to formation of silicon containing polymers. In one embodiment of the invention, the prepolymer includes a compound, or any combination of compounds, denoted by Formula I:

$$Rx - Si - Ly \qquad \text{(Formula I)}$$

wherein x is an integer ranging from 0 to about 2 and y is 4-x, an integer ranging from about 2 to about 4),

R is independently alkyl, aryl, hydrogen, alkylene, arylene and/or combinations of these,

L is independently selected and is an electronegative group, e.g., alkoxy, carboxyl, amino, amido, halide, isocyanato and/or combinations of these.

Particularly useful prepolymers are those provided by Formula I when x ranges from about 0 to about 2, y ranges from about 2 to about 4, R is alkyl or aryl or H, and L is an electronegative group, and wherein the rate of hydrolysis of the Si-L

bond is greater than the rate of hydrolysis of the Si-OCH_2CH_3 bond. Thus, for the following reactions designated as (a) and (b):

(a) Si-L + H_2O → Si-OH + HL

(b) Si-OCH_2CH_3 + H_2O → Si-OH + $HOCH_2CH_3$

The rate of (a) is greater than rate of (b).

Examples of suitable compounds according to Formula I include, but are not limited to:

$Si(OCH_2CF_3)_4$	tetrakis(2,2,2-trifluoroethoxy)silane,
$Si(OCOCF_3)_4$	tetrakis(trifluoroacetoxy)silane*,
$Si(OCN)_4$	tetraisocyanatosilane,
$CH_3Si(OCH_2CF_3)_3$	tris(2,2,2-trifluoroethoxy)methylsilane,
$CH_3Si(OCOCF_3)_3$	tris(trifluoroacetoxy)methylsilane*,
$CH_3Si(OCN)_3$	methyltriisocyanatosilane,

[* These generate acid catalyst upon exposure to water]
and or combinations of any of the above.

In another embodiment of the invention, the composition includes a polymer synthesized from compounds denoted by Formula I by way of hydrolysis and condensation reactions, wherein the number average molecular weight ranges from about 150 to about 300,000 amu, or more typically from about 150 to about 10,000 amu.

In a further embodiment of the invention, silicon-containing prepolymers useful according to the invention include organosilanes, including, for example, alkoxysilanes according to Formula II:

$$
\begin{array}{c} R \\ | \\ R\text{-}Si\text{-}R \\ | \\ R \end{array} \qquad \text{Formula II}
$$

Optionally, Formula II is an alkoxysilane wherein at least 2 of the R groups are independently C_1 to C_4 alkoxy groups, and the balance, if any, are independently selected from the group consisting of hydrogen, alkyl, phenyl, halogen, substituted phenyl. For purposes of this invention, the term alkoxy includes any other organic groups which can be readily cleaved from silicon at temperatures near room temperature by hydrolysis. R groups can be ethylene glycoxy or propylene glycoxy or the like, but preferably all four R groups are methoxy, ethoxy, propoxy or butoxy. The most preferred alkoxysilanes nonexclusively include tetraethoxysilane (TEOS) and tetramethoxysilane.

In a further option, for instance, the prepolymer can also be an alkylalkoxysilane as described by Formula II, but instead, at least 2 of the R groups are independently C_1 to C_4 alkylalkoxy groups wherein the alkyl moiety is C_1 to C_4 alkyl and the alkoxy moiety is C_1 to C_6 alkoxy, or ether-alkoxy groups; and the balance, if any, are independently selected from the group consisting of hydrogen, alkyl, phenyl, halogen, substituted phenyl. In one preferred embodiment each R is methoxy, ethoxy or propoxy. In another preferred embodiment at least two R groups are alkylalkoxy groups wherein the alkyl moiety is C_1 to C_4 alkyl and the alkoxy moiety is C_1 to C_6 alkoxy. In yet another preferred embodiment for a vapor phase precursor, at least two R groups are ether-alkoxy groups of the formula (C_1 to C_6 alkoxy)$_n$ wherein n is 2 to 6.

Preferred silicon-containing prepolymers include, for example, any or a combination of alkoxysilanes such as tetraethoxysilane, tetrapropoxysilane,

tetraisopropoxysilane, tetra(methoxyethoxy)silane, tetra(methoxyethoxyethoxy)silane which have four groups which may be hydrolyzed and than condensed to produce silica, alkylalkoxysilanes such as methyltriethoxysilane silane, arylalkoxysilanes such as phenyltriethoxysilane and precursors such as triethoxysilane which yield SiH functionality to the film. Tetrakis(methoxyethoxyethoxy)silane, tetrakis(ethoxyethoxy)silane, tetrakis(butoxyethoxyethoxy)silane, tetrakis(2-ethylthoxy)silane, tetrakis(methoxyethoxy)silane, and tetrakis(methoxypropoxy)silane are particularly useful for the invention.

In a still further embodiment of the invention, the alkoxysilane compounds described above may be replaced, in whole or in part, by compounds with acetoxy and/or halogen-based leaving groups. For example, the prepolymer may be an acetoxy (CH_3-CO-O-) such as an acetoxy-silane compound and/or a halogenated compound, e.g., a halogenated silane compound and/or combinations thereof. For the halogenated prepolymers the halogen is, e.g., Cl, Br, I and in certain aspects, will optionally include F. Preferred acetoxy-derived prepolymers include, e.g., tetraacetoxysilane, methyltriacetoxysilane and/or combinations thereof.

In one particular embodiment of the invention, the silicon containing prepolymer includes a monomer or polymer precursor, for example, acetoxysilane, an ethoxysilane, methoxysilane and/or combinations thereof.

In a more particular embodiment of the invention, the silicon containing prepolymer includes a tetraacetoxysilane, a C_1 to about C_6 alkyl or aryl-triacetoxysilane and combinations thereof. In particular, as exemplified below, the triacetoxysilane is a methyltriacetoxysilane.

The silicon containing prepolymer is usually present in the overall composition in an amount of from about 10 weight percent to about 80 weight percent, and more usually present in the overall composition in an amount of from about 20 weight percent to about 60 weight percent.

For non-microelectronic applications, the onium or nucleophile catalyst may contain metal ions. Examples include sodium hydroxide, sodium sulfate, potassium hydroxide, lithium hydroxide, and zirconium containing catalysts.

For microelectronic applications, the composition then may optionally contain at least one metal-ion-free catalyst which is an onium compound or a nucleophile. The catalyst may be, for example an ammonium compound, an amine, a phosphonium compound or a phosphine compound. Non-exclusive examples of such include tetraorganoammonium compounds and tetraorganophosphonium compounds including tetramethylammonium acetate, tetramethylammonium hydroxide, tetrabutylammonium acetate, triphenylamine, trioctylamine, tridodecylamine, triethanolamine, tetramethylphosphonium acetate, tetramethylphosphonium hydroxide, triphenylphosphine, trimethylphosphine, trioctylphosphine, and combinations thereof. The composition may comprise a non-metallic, nucleophilic additive which accelerates the crosslinking of the composition. These include dimethyl sulfone, dimethyl formamide, hexamethylphosphorous triamide (HMPT), amines and combinations thereof. The catalyst is usually present in the overall composition in an amount of from about 1 ppm by weight to about 1000 ppm, and more usually present in the overall composition in an amount of from about 6 ppm to about 200 ppm.

The overall composition then optionally includes a solvent composition. Reference herein to a "solvent" should be understood to encompass a single

solvent, polar or nonpolar and/or a combination of compatible solvents forming a solvent system selected to solubilize the overall composition components. A solvent is optionally included in the composition to lower its viscosity and promote uniform coating onto a substrate by art-standard methods.

In order to facilitate solvent removal, the solvent is one which has a relatively low boiling point relative to the boiling point of the precursor components. For example, solvents that are useful for the processes of the invention have a boiling point ranging from about 50 °C to about 250 °C to allow the solvent to evaporate from the applied film and leave the active portion of the precursor composition in place. In order to meet various safety and environmental requirements, the solvent preferably has a high flash point (generally greater than 40 °C) and relatively low levels of toxicity. A suitable solvent includes, for example, hydrocarbons, as well as solvents having the functional groups C-O-C (ethers), -CO-O (esters), -CO- (ketones), -OH (alcohols), and –CO-N-(amides), and solvents which contain a plurality of these functional groups, and combinations thereof.

Suitable solvents for use in such solutions of the present compositions include any suitable pure or mixture of organic, organometallic, or inorganic molecules that are volatized at a desired temperature. Suitable solvents include aprotic solvents, for example, cyclic ketones such as cyclopentanone, cyclohexanone, cycloheptanone, and cyclooctanone; cyclic amides such as N-alkylpyrrolidinone wherein the alkyl has from about 1 to 4 carbon atoms; and N-cyclohexylpyrrolidinone and mixtures thereof. A wide variety of other organic solvents may be used herein insofar as they are able to aid dissolution of the adhesion promoter and at the same time effectively control the viscosity of the resulting solution as a coating solution. Various facilitating measures such as

stirring and/or heating may be used to aid in the dissolution. Other suitable solvents include methyethylketone, methylisobutylketone, dibutyl ether, cyclic dimethylpolysiloxanes, butyrolactone, γ-butyrolactone, 2-heptanone, ethyl 3-ethoxypropionate, 1-methyl-2-pyrrolidinone, and propylene glycol methyl ether acetate (PGMEA), and hydrocarbon solvents such as mesitylene, xylenes, benzene, toluene di-n-butyl ether, anisole, acetone, 3-pentanone, 2-heptanone, ethyl acetate, n-propyl acetate, n-butyl acetate, ethyl lactate, ethanol, 2-propanol, dimethyl acetamide, propylene glycol methyl ether acetate, and/or combinations thereof. It is better that the solvent does not react with the silicon containing prepolymer component.

The solvent component may be present in an amount of from about 10 % to about 95 % by weight of the overall composition. A more usual range is from about 20 % to about 75 % and most usually from about 20 % to about 60 %. The greater the percentage of solvent employed, the thinner is the resulting film.

In another embodiment of the invention the composition may comprises water, either liquid water or water vapor. For example, the overall composition may be applied to a substrate and then exposed to an ambient atmosphere that includes water vapor at standard temperatures and standard atmospheric pressure. Optionally, the composition is prepared prior to application to a substrate to include water in a proportion suitable for initiating aging of the precursor composition, without being present in a proportion that results in the precursor composition aging or gelling before it can be applied to a desired substrate. By way of example, when water is mixed into the precursor composition it is present in a proportion wherein the composition comprises water in a molar ratio of water to Si atoms in the silicon containing prepolymer ranging from about

0.1:1 to about 50:1. A more usual range is from about 0.1:1 to about 10:1 and most usually from about 0.5:1 to about 1.5:1.

Those skilled in the art will appreciate that specific temperature ranges for crosslinking from the dielectric films will depend on the selected materials, substrate and desired structure, as is readily determined by routine manipulation of these parameters. Generally, the coated substrate is subjected to a treatment such as heating to effect crosslinking of the composition on the substrate to produce a gelled film.

Crosslinking may be done in step (c) by heating the film at a temperature ranging from about 100 °C to about 250 °C, for a time period ranging from about 30 seconds to about 10 minutes to gel the film. The artisan will also appreciate that any number of additional art-known curing methods are optionally employed, including the application of sufficient energy to cure the film by exposure of the film to electron beam energy, ultraviolet energy, microwave energy, and the like, according to art-known methods.

Once the film has aged, i.e., once it is is sufficiently condensed to be solid or substantially solid, the gelled film is heated. Heating the gelled film is done at a temperature of from about 750 °C to about 1000 °C and for a duration effective to remove substantially all organic moieties and to produce a substantially crack-free silica dielectric film. More usually, heating is conducted at a temperature of from about 900 °C to about 1000 °C. The heating may be conducted for from about 30 minutes to about 120 minutes, or more usually for a time period ranging from about 45 minutes to about 75 minutes. In one embodiment, the step (c) crosslinking is conducted at a temperature which is less than the heating temperature of step (d).

The overall composition may also comprise additional components such as adhesion promoters, antifoam agents, detergents, flame retardants, pigments, plasticizers, stabilizers, and surfactants. The composition also has utility in non-microelectronic applications such as thermal insulation, encapsulant, matrix materials for polymer and ceramic composites, light weight composites, acoustic insulation, anti-corrosive coatings, binders for ceramic powders, and fire retardant coatings.

The present composition is particularly useful in microelectronic applications as a dielectric substrate material in microchips, multichip modules, laminated circuit boards, or printed wiring boards. The composition may also be used as an etch stop or hardmask.

The present composition may be used in electrical devices and more specifically, as an interlayer dielectric in an interconnect associated with a single integrated circuit ("IC") chip. An integrated circuit chip typically has on its surface a plurality of layers of the present composition and multiple layers of metal conductors. It may also include regions of the present composition between discrete metal conductors or regions of conductor in the same layer or level of an integrated circuit.

The method of the invention is suitable for forming isolation structures in a semiconductor substrate, such as shallow trench isolation structures. In so doing, one may begin by etching trenches in a semiconductor substrate, thereby forming substantially unetched areas of said substrate between the trenches. Thereafter the composition of the invention is deposited and conformally fills the trenches and forms a film. Crosslinking of the composition follows to produce a gelled film. The gelled film is then heated at a temperature of from about 750 °C to

about 1000 °C and for a duration effective to remove substantially all organic moieties and to produce a substantially crack-free silica dielectric film. Optionally the silica dielectric film is planarized such as by chemical mechanical polishing under conditions well known in the art. Excellent void free gap-fill performance can be expected down to 0.01 μm and beyond. Gap-fill capability of high aspect ratio structures can be extended beyond 30:1. The films have excellent wet etch resistance having a wet etch removal rate of from about 30 angstroms/minute to about 400 angstroms/minute when immersed in a diluted HF-water (100:1 volume : volume ratio) for a period of 10 minutes.

The following non-limiting examples serve to illustrate the invention.

EXAMPLE 1

This example shows the production of a silicon-containing pre-polymer. A precursor was prepared by combining 1300 g tetraacetoxysilane, 1300 g methyltriacetoxysilane, and 1400 g propylene glycol methyl ethyl acetate (PGMEA) in a 6 liter reactor containing a overhead stirrer and a jacketed water cooler. These ingredients were weighed out within an N_2-environment (N_2 glove bag). The reactor was also connected to an N_2 environment to prevent environmental moisture from entering the solution (standard temperature and pressure).

The reaction mixture was heated to 80 °C before 194.8 g of water was added to the flask at a rate of 16 ml/minute. After the water addition is complete, the reaction mixture was allowed to cool to ambient before it was filtered through a 0.2 micron filter to provide the precursor solution for the next step. The solution is then deposited onto a series of 8-inch silicon wafers, each on a spin chuck and

spun at 1000 rpm for 15 seconds. The presence of water in the precursor resulted in the film coating being substantially condensed by the time that the wafer was inserted into the first oven. Insertion into the first oven, as discussed below, takes place within the 10 seconds of the completion of spinning. Each coated wafer was then transferred into a sequential series of ovens preset at specific temperatures, for one minute each. In this example, there are three ovens, and the preset oven temperatures were 125°C, 200°C, and 350°C, respectively. Each wafer is cooled after receiving the three-oven stepped heat treatment, and the produced dielectric film was measured using ellipsometry to determine its thickness and refractive index. The baked film is also heated at a higher temperature to remove substantially all organic moieties and to produce a substantially crack-free silica dielectric film for further characterizations. Each wafer is weighed to allow for gravimetric analysis to determine its film density. A small piece of the film-coated wafer is also subjected to wet etch rate analysis. The film-coated wafer piece is immersed in a diluted HF-water (100:1 volume : volume ratio) for a period of 10 minutes. The difference in film thickness divided by the wet etch time (10 min) provides the wet etch rate (WER) of a given film in the 100:1 HF-water solution. PECVD TEOS oxide film is also subjected to this wet etch test to provide a reference for the films.

EXAMPLE 2

Each film-coated wafer is then further cured at 800 °C for one hour under flowing nitrogen. A non-porous film made from the liquid precursor of this invention will have a density of 2.04 ± 0.09. The film has a bake thickness of 7674 Å, a bake density of 1.41, a cure thickness of 6043 Å and a cure density of 2.04 ± 0.09. WER of film cured at 800 °C is calculated to be at 133 Å/min. In comparison, PECVD silicon oxide has a density of 2.25 g/mL, and a WER of 72 Å/min.

EXAMPLE 3

Each film-coated wafer is alternatively cured at 1000 °C for one hour under flowing nitrogen. A non-porous film made from the liquid precursor of this invention will have a density of 2.30 ± 0.09. The film has a bake thickness of 7674 Å, a bake density of 1.41, a cure thickness of 4944 Å and a cure density of 2.30 ± 0.09. WER of film cured at 1000 °C is calculated to be at 30 Å/min. In comparison, PECVD silicon oxide has a density of 2.25 g/mL, and a WER of 72 Å/min.

While the present invention has been particularly shown and described with reference to preferred embodiments, it will be readily appreciated by those of ordinary skill in the art that various changes and modifications may be made without departing from the spirit and scope of the invention. It is intended that the claims be interpreted to cover the disclosed embodiment, those alternatives which have been discussed above and all equivalents thereto.